Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A logic development system using an external microcomputer which replaces a built-in microcomputer incorporated in an existing electronic control unit, comprising:

a mother board including an application block and a first communication block;

a core board including one or more devices which simulate, by software, peripheral devices of the built-in microcomputer so as to execute an input or output process, the core board further including a computing block and a second communication block;

a peripheral component interconnect (PCI) bus coupling said mother board and said core board; and

an interface board including a port assignment conversion board, a plurality of standard circuits, and a plurality of facility boards which are associated with hardware of said electronic control unit, said standard circuits and facility boards being selectable by said port assignment conversion board, and said port assignment conversion board being ~~wherein the interface board is~~ coupled to said core board ~~one or more devices~~ via a harness, wherein:

said first communication block included in said mother board and each of said one or more devices included in said core board are coupled to each other over said PCI bus; and

said communication block and each of said one or more devices transfer data to or from each other over said PCI bus.

2. (Currently Amended) A logic development system using an external microcomputer which replaces a built-in microcomputer incorporated in an existing electronic control unit, comprising:

a mother board including an application block and a first communication block;

a core board including one or more devices which simulate, by software, peripheral devices of the built-in microcomputer so as to execute an input or output process, the core board further including a computing block and a second communication block;

a peripheral component interconnect (PCI) bus coupling said mother board and said core board;

an interface board including a port assignment conversion board, a plurality of standard circuits, and a plurality of facility boards which are associated with hardware of said electronic control unit, said standard circuits and facility boards being selectable by said port assignment conversion board, and said port assignment conversion board being ~~wherein the interface board is~~ coupled to said core board ~~one or more devices~~ via a harness[[,]]; and[[:]]

a bus controller in said computing block interposed between said first communication block in said mother board and each of said one or more devices[[;]], wherein,

said first communication block included in said mother board and said bus controller are coupled to each other over said PCI bus, and said bus controller and each of said one or more devices are coupled to each other over an internal bus[[;]], and

said first communication block and each of said one or more devices transfer data to or from each other by way of said PCI bus, bus controller, and internal bus.

3. (Currently Amended) A microcomputer logic development system according to claim 1, wherein: a virtual memory device is interposed between said first communication block included in said mother board and said PCI bus; and when transfer data is temporarily recorded in said virtual memory device ~~at the timing of~~ in response to receiving or transmitting data, said virtual memory device behaves like a memory device included in the built-in microcomputer.

4. (Previously Presented) A microcomputer logic development system according to claim 1, wherein: an object on which said application block acts is a vehicle; said logic development system includes an ignition switch; and when said logic development system is interlocked with an on or off state of said ignition switch, control software for said vehicle is

initiated or terminated in the same manner as control software residing in said electronic control unit.

5. (Currently Amended) A microcomputer logic development system according to claim 4, wherein said ~~circuits that are included in said interface board and associated with the hardware of said electronic control unit include at~~ plurality of facility boards includes at least one facility circuit in which a microcomputer is incorporated; and said facility circuit is not actuated with the on state of said ignition switch but is actuated synchronously with starting up of the mother board.

6. (Previously Presented) A microcomputer logic development system according to claim 5, wherein said facility circuit includes a power circuit that is actuated with the on state of said ignition switch, and a logic circuit which actuates the microcomputer in the facility circuit when both a signal sent from said power circuit and a signal sent from said mother board become valid.

7. (Currently Amended) A microcomputer logic development system according to claim 4, wherein: when said ignition switch is turned off, data that should be held is stored in either of a memory included in an external storage device coupled to said logic development system or a memory included in said logic development system; when said ignition switch is turned on, data that should be held is read from said external storage device and restored; and [[the]] a same capability as the capability of a backup memory is thus realized for said logic development system.

8. (Currently Amended) A microcomputer logic development system according to claim 4, wherein initial values to ports are set within an initialization routine which is executed on said mother board when said ignition switch is turned on after [[the]] a power supply of said logic development system is turned on.

9. (Currently Amended) A microcomputer logic development system according to claim 1, wherein: said PCI bus contains a one-channel interrupt signal line over which an interrupt request is issued from said core board to said mother board; when said interrupt signal line is activated by said core board, said application block included in said mother board accepts [[an]] the interrupt request; and after the interrupt request is accepted, said interrupt signal line is inactivated.

10. (Previously Presented) A microcomputer logic development system according to claim 9, wherein when interrupt handling is terminated, said application block included in said mother board checks if said interrupt signal line is inactive.

11. (Previously Presented) A microcomputer logic development system according to claim 10, wherein when interrupt handling is terminated, if said interrupt signal line is active, said application block included in said mother board inactivates said interrupt signal line.

12. (Previously Presented) A microcomputer logic development system according to claim 1, wherein: said computing block included in said core board includes a facility for temporarily fetching data; when a large amount of data is transferred between said mother board and each of said one or more devices included in said core board, the large amount of data is transferred in a burst mode between said mother board and said computing block, and transferred in a non-burst mode between said computing block and each of said one or more devices.

13. (Previously Presented) A microcomputer logic development system according to claim 9, wherein after said application block included in said mother board accepts an interrupt request, said application block acquires interrupt flags from each of said one or more devices over said PCI bus; after said application block acquires interrupt flags, said application block clears the interrupt flags present in each of said one or more devices.

14. (Previously Presented) A microcomputer logic development system according to claim 13, wherein after said application block included in said mother board acquires interrupt flags, said application block executes a process associated with each of the acquired interrupt flags.

15. (Previously Presented) A microcomputer logic development system according to claim 9, wherein: after said application block included in said mother board accepts an interrupt request, said application block acquires a plurality of interrupt flags from each of said one or more devices over said PCI bus; said application block selects one interrupt flag assigned a high priority, and executes a process associated with the interrupt flag; and after the process is completed, said application block clears a process completion interrupt flag present in each of said one or more devices.

16. (Currently Amended) A microcomputer logic development system according to claim 15, wherein after said application block selects one interrupt flag assigned a high priority, and executes a process associated with the interrupt flag, said application block re-acquires a plurality of interrupt flags from each of said one or more devices over said PCI bus.

17. (Previously Presented) A microcomputer logic development system according to claim 13, wherein said interrupt flags are concurrently stored at successive addresses in one of one or more registers included in each of said one or more devices.

18. (Currently Amended) A microcomputer logic development system according to claim 17, wherein: a plurality of core boards are included; interrupt flags representing interrupts caused by each of a plurality of resources that are included in each of said core boards are stored in a register included in each of said core boards; the interrupt flags representing interrupts caused by each of the resources included in [[the]] a first one of the plurality of core boards are stored in the register included in the first one of the plurality of core boards; and an extension interrupt flag indicating whether interrupt flags, representing interrupts caused by each of the

resources included in each ~~of the~~ remaining ones of the plurality of core boards, are present is stored in association with each core board.

19. (Previously Presented) A microcomputer logic development system according to claim 18, wherein if said extension interrupt flag demonstrates that interrupt flags are stored in the register included in any of the remaining core boards, said application block acquires the interrupt flags from the register in the remaining core board.

20. (Currently Amended) A microcomputer logic development system according to claim 1, wherein: a plurality of core boards are included; the first one of the plurality of core boards alone includes a free-run timer; said first one of the plurality of core boards includes at least resources that act synchronously with [[the]] a timer value of said free-run timer; and [[the]] remaining ones of the plurality of core boards include resources independent of said free-run timer.

21. (Original) A microcomputer logic development system according to claim 20, wherein: the resources that act synchronously with the timer value of said free-run timer include a comparator and a capture unit; and the resources independent of said free-run timer include a pulse-width modulator (PWM), a communication unit, an A/D converter, and ports.

22. (Currently Amended) A logic development system using an external microcomputer which replaces a built-in microcomputer incorporated in an existing electronic control unit, comprising:

a mother board including an application block;

a core board including one or more devices which simulate, by software, peripheral devices of the built-in microcomputer so as to execute an input or output process; [[and]]

a peripheral component interconnect (PCI) bus over which said mother board and said core board are coupled to each other~~, wherein:~~; and

an interface board that includes a port assignment conversion board, a plurality of standard circuits, and a plurality of facility boards which are associated with hardware of said electronic control unit, said standard circuits and facility boards being selectable by said port assignment conversion board, and said port assignment conversion board being coupled to said core board via a harness, wherein:

when an interrupt factor occurs in any of said one or more devices, said application block reads or writes data in or from said one or more devices; and

data whose processing speed is requested to be low is read or written all together during communication performed before or after action of said application block.

23. (Currently Amended) A logic development method for a microcomputer including a mother board having an application block, a core board having one or more devices which simulate, by software, peripheral devices of the built-in microcomputer so as to execute an input or output process, an interface board having a port assignment conversion board, a plurality of standard circuits, and a plurality of facility boards which are associated with hardware of an electronic control unit, said standard circuits and facility boards being selectable by said port assignment conversion board, and said port assignment conversion board being coupled to said core board via a harness, and a peripheral component interconnect (PCI) bus over which said mother board and said core board are coupled to each other, said microcomputer logic development method comprising:

issuing an interrupt request from said core board to said mother board over a one-channel interrupt signal line contained in said PCI bus;

accepting the interrupt request when said interrupt signal line is activated via said core board; and

inactivating said interrupt signal line after the interrupt request is accepted.

24. (Previously Presented) A microcomputer logic development method according to claim 23, further comprising the steps of:

after an interrupt request is accepted, acquiring interrupt flags from each of said one or more devices over said bus; and

after the interrupt flags are acquired, clearing the interrupt flags from each of said one or more devices.

25. Canceled.

26. (New) The microcomputer logic development system of claim 2, wherein the motherboard includes a first central processing unit, and the core board includes a second central processing unit.

27. (New) The microcomputer logic development system of claim 2, wherein each of the plurality of facility boards include a microcomputer for transferring data to and from the one or more devices.

28. (New) The microcomputer logic development system of claim 27, wherein the transferring of data to and from the one or more devices is based on a direct memory access technique.

29. (New) The method of claim 23, wherein each of the plurality of facility boards include a microcomputer, and the method further comprises:

transferring data to and from the one or more devices via the microcomputer.